ABSTRACT

The invention is directed to reducing of the number of steps in a BiCMOS process. A first N-well 3A and a second N-well 3B are formed deeply on a surface of a P-type semiconductor substrate. A first P-well 4A is formed in the first N-well 3A, and an N-channel MOS transistor is formed in the first P-well 4A. The second N-well 3B is used as a collector of a vertical NPN bipolar transistor. A second P-well 4B is formed in the second N-well 3B. The second P-well 4B is formed simultaneously with the first P-well 4A. The second P-well 4B is used as a base of the vertical NPN bipolar transistor. An N+ emitter layer and a P+ base electrode layer of the vertical NPN bipolar transistor are formed on a surface of the second P-well 4B.